PATENT APPLICATION
Docket No. 5038-358

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chuan Hu and Daoqiang Lu

Assignee:	Intel Corporation	Confirmation No. 3995
Serial No.:	10/797,755	Examiner: Owens, Douglas W.
Filed:	March 9, 2004	Group Art Unit: 2811
For:	FLUXLESS DIE-TO-HEAT SPREADER BONDING USING THERMAL INTERFACE MATERIAL	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION TO OVERCOME A CITED PUBLICATION
37 C.F.R. §1.131

1. The persons making this Declaration are Chuan Hu and Daoqiang Lu, inventors of the above-referenced patent application ("Application").

2. Certain claims of U.S. Patent Application No. 10/797,755 are currently rejected in view of certain prior art, *inter alia*, U.S. Patent Application Publication No. 2004/0099932 to Elliott, et al. Elliott has a filing date ("Effective Date") of November 27, 2002.

3. Conception of the invention that is the subject of the claims in the present application occurred prior to the Effective Date of the Elliott patent application as evidenced by the attached Invention Disclosure document (Exhibit A) submitted internally at Intel prior to the Elliott filing date of November 27, 2002.

4. Work on the invention was conducted continuously from a date prior to the Effective Date, until the date of filing of the above referenced patent application, and thereafter.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Chuan Hu

Dated: 04/06/05

Daoqiang Lu

Dated: 4/6/05

INTEL CONFIDENTIAL
Attorney-Client Privileged Communication

29365

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TMG INVENTION DISCLOSURE

Located at: http://legal.intel.com

TMG-TM/TMG/ATD

LEGAL ID# _____(legal dept. use only) DATE: _____

It is important to provide accurate and detailed information on this form (fill in ALL areas under Inventor[s]). The information will be used to evaluate your invention for possible filing as a patent application. When completed, please return this form to **Janice Boulden, Intel Legal Department at JF3-147. You can submit electronically via e-mail to "invention disclosure submission" if all of the information is electronic, including drawings and supervisor approval.** If you have any questions regarding this form or to whom it should be forwarded, please call **503-264-0444**.

Fill out the below and follow the instructions:

1. Field of the Invention:

- Semiconductor Process: device and integration
- Semiconductor Process + Equipment: thin films
- Semiconductor Process + Equipment: etch/litho
- Circuit Design
- Flash
- Test
- CQN (Q&R)
- X Packaging
  - Boards/Cartridge
  - Automation
- Other

2. Concise Title of Invention:

Fluxless die to IHS bonding of TDTT (thin die thin TIM) package using thin AuSn TIM and N2 purged reflow oven

EXHIBIT
tabbies
A

3. **Brief Description of Invention (please use only space provided and font #10 or larger. Write the Key Elements of the Invention AND EXPLAIN HOW YOU DETECT INFRINGEMENT):**

The invention is:

a manufacturable fluxless bonding method of TDTT package. It has been proven experimentally that the TDTT package is capable of delivering thermal performance for P1266 and is scalable for generations beyond. The AuSn solder TIM die/IHS bonding has been verified experimentally to be with very good reliability. However, the previous bonding methods were in H2 purged furnace or in formic acid vapor ambient, which are expansive, with low throughput and not compatible with the equipment used for earlier generations (P1262 and P1264). The bonding process proposed in this invention is conducted in a conventional reflow oven, which is purged with N2.

The key elements are:

- A manufacturable fluxless bonding method for TDTT packages with high throughput and compatibility with POR equipments used for other solder TIM bonding. This is a method that can be used for HVM.
- The TDTT package with this solder TIM1 can deliver thermal solution for P1266 microprocessors and beyond.
- No surface treatment is needed for this process, which is also cost saving.
- A fluxless bonding method for cost saving and void reduction.
- The bonding is processed in standard N2 purged reflow oven 10 zones.
- The solder is plated or evaporated on IHS. No preform is used. Thus the bonding process is simplified.

4. Inventor(s):

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Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR_X__
STTD___ CQN ___
SMTD___TCAD___
Other?_____
Contractor:
YES _____
NO ____X___
Inventor Signature:

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Division Name: ATD___
PTD___ CTM___ CR_x__
STTD___ CQN ___
SMTD___TCAD___
Other?_____
Contractor:
YES _____
NO ____x___
Inventor Signature:

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Citizenship:
Supervisor Name:
Supervisor Phone:
Supervisor M/S:

Group Name: TMG
Division Name: ATD___
PTD___ CTM___ CR___
STTD___ CQN ___
SMTD___TCAD___
Other?_____
Contractor:
YES _____
NO _____
Inventor Signature:

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

5. **HAVE YOUR SUPERVISOR READ, DATE AND SIGN COMPLETED FORM (use first inventor's supervisor if multiple inventors)**

DATE: Sept. 27, 2002 **SUPERVISOR NAME:** Gilroy Vandentop

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID.

6. **Has subject matter of present disclosure been disclosed or will it be disclosed outside Intel?**
If yes, explain and give date: No
(Give expected tape out date if applicable):

7. **Has the subject matter of present disclosure been published or will it be published outside of Intel?**
If yes, explain and give date: No

8. **Has a product using or manufactured using the present disclosure been sold or offered for sale?**
If yes, explain and give date: No

9. **Has this invention been conceived, or constructed during accomplishment of a government or third party contract? If yes, give contract name and number:** No

10. **Explain the problem being addressed by the invention:**

This invention addresses the problem of:

- Thermal performance requirement gap between P1264 and P1266. Soft solder based TIMs cannot bond die and IHS reliably if the TIM thickness is small. It cannot deliver thermal performance for P1266 with thick TIM.
- Low throughput and high cost of other fluxless die/IHS bonding methods (like H2, formic acid vapor, forming gas...) for TDTT.
- TIM bonding with fluxes generate voids which cause reliability issues

11. **Explain current state of the art (i.e, how the problem is solved today):**

There is no solution that can meet Rjc requirement of P1266 now. No package currently used can deliver the thermal performance needed for P1266.
The state of art die to IHS bonding method uses flux and soft solder preform around 200 um as the TIM material

12. **Explain technical advantages of the invention over current state of the art:**

The technical advantage of this invention is:
The proposed fluxless solder TIM1 bonding process using a lead-free solder (AuSn) in N2 purged conventional reflow oven for TDTT packages can offer following advantages:

1. Manufacturability. This approach is an in-line process and compatible with the POR equipment used for processes of earlier generations. This is a method that can be used in HVM. N2 purged ambient is the standard option of reflow oven. And the higher processing temperature can be achieved in many commercially available systems.
2. High thermal performance. Fluxless bonding process will provide a very thin, uniform and void-free TIM joint and thus provide TDTT package with a high thermal performance.
3. Simpler bonding process, high throughput and low cost. Flux-related processing steps are eliminated. Also, solder perform handling is eliminated because no perform is used.

13. a. **Is the invention experimentally verified?** Yes
    b. **Is the invention verified with simulation?** Yes
    c. **If neither a. or b. above, then you can get a patent on the concept, but please explain the technical basis to justify that your invention will work (use extra space if necessary):**

14. **Detailed Description of Invention (try to use only the space provided with font #10 or larger type. Refer to your drawings):**

Processing of this package.

1. The wafer is thinned to about 50 to 150 um. Then the wafer backside metallization (BSM), such as 100nmTi / 100nmNiV / 1000nmAu, is deposited. The wafer can be diced during the thinning process or after thinning. Certain kind of support like transparent glass with UV sensitive epoxy might be used to support the thinned die/wafer.

Figure 1 Thinning, BSM deposition, dicing of a wafer

2. Multi layers of intermetallic solder components are deposited on flat IHS using E-plating or other methods as shown in Figure 2. (3 um Ni/ 3 um Au /3 um Sn)

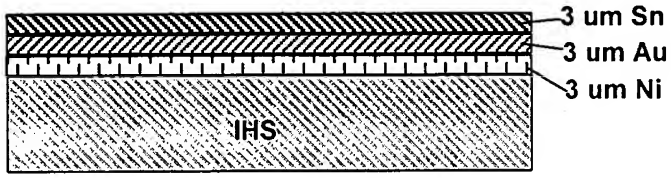

Figure 2: metalization on IHS. Either multilayer of solder components with thickness as shown above is deposited on IHS.

3. Die and IHS are pressed together using bonding clip and load into reflow oven purged with N2. The actual processing temperature in TIM is heated to above 300 ° C for 2 to 3 minutes. The ramp down rate should be lower than 100 C/minute. Several cooling zones with small temperature gradient are needed to prevent die from cracking due to CTE mismatch. Many other ways to bond the front side of die on substrate to make a complete package have been reported in our previous IDFs.

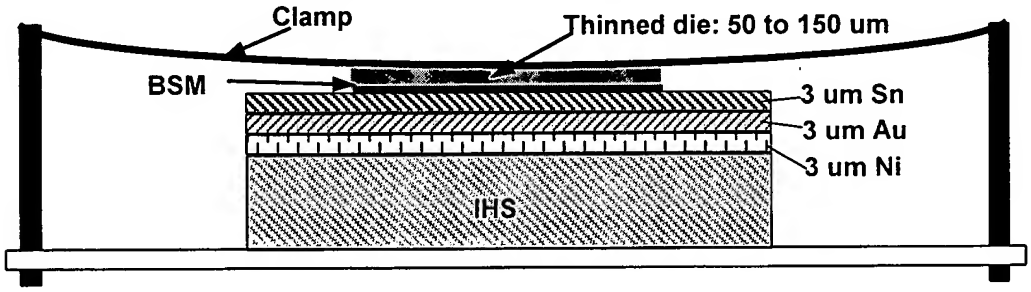

Figure 3: Die and IHS is pressed together using a clip and loaded into N2 purged reflow oven for bonding.

Drawings (use as many pages as needed)
(PLEASE DO NOT MAKE COLOR DRAWINGS)

16. Key Supporting Data (1 page limit on separate page):

Experimental evidence (Bonding):

1. CSAM:
   no detectable voids were found in the TIM layer.
2. Shear Test:
   The bonded 1cmx1cm die shows a 58.2 Kg shear force when it was sheared off partially from IHS. Visual inspection indicates that the debonding happens primarily within TIM layer, which suggests a good bonding on die and IHS.

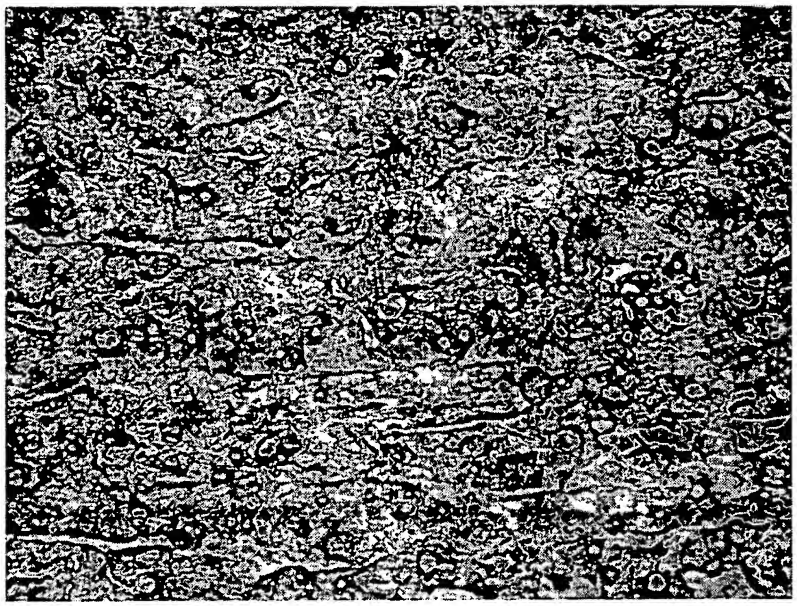

Fig. 4: The surface of the debonding region on IHS after shear test. Rough intermetallic surface indicates that debonding happens on at AuSn TIM layer and a good bonding is achieved.

3. Thermal measurement:
In our previous study, the TDTT package with 50 um die and 6 um TIM survived 500 TCB with no detectable change on CSAM images. And laser flash measurement shows the total Rjc for TDTT package could be as low as 0.069 C cm^2/W, which is lower than PX68 thermal target.

Simulation result of thermal performance gain of TDTT package has been reported in patent (Filing #12660, "THINNED DIE INTEGRATED CIRCUIT PACKAGE"). In summary, the TDTT package has a potential 28% to 35% junction to ambient thermal performance gain over P1264 package with solder TIM1.

17. What is the product or process invention to be used on? (e.g., P8xx, name of product, etc.):
P1266 and beyond

18. Have you reviewed your invention with a TMG Patent Mentor? (see below for mentor names) If so, give name: _____

19. Any other information the IP Committee should consider?
The TDTT project has shown great potential and it has relatively poor IP protection so far. More of less some kind of TDTT is a must for future product.

MENTOR REVIEW

If you don't already have a departmental peer review process for invention disclosures, we recommend you have it reviewed by a Mentor before you send your invention disclosure to Intel Legal. The purpose of this Mentor review is to ensure that the invention disclosure is written clearly enough for the IP Committee to comprehend your invention

including all the novel aspects of it. Please refer to the list below for recommended Mentors by area. Select ONE Mentor to review and acknowledge. This recommended step is not meant to unreasonably slow down the invention disclosure process. If your Mentor fails to respond to you in a reasonable amount of time, then send your invention disclosure directly to Intel Legal.

AREA OF EXPERTISE	MENTOR NAME
Semiconductor Process-device and integration	Mark Bohr, Robert Chau, Krishna Seshan
Semiconductor Process-thin films	Ken Cadien, Chien Chiang
Semiconductor Process-etch/litho	Peter Silverman, Peter Charvat (etch), Yan Borodovsky (litho), George Chen (litho)
Fab Process Equipment	Maciek Orczyk
Circuits Design	Ian Young, Greg Taylor, Clair Webb, Rajesh Galivanche
Flash	Manzur Gill, Krishna Seshan
Test	J.J. Grealish, Rajesh Galivanche, Mike Mayberry
CQN (Q&R)	Ian Young, Greg Taylor, Clair Webb, Valluri (Bob) Rao
Packaging	Bob Sankman, Rama Shukula
Boards/Cartridge	Terry Dishongh
Automation	Sunit Rikhi
Optical and MEMS	Valluri (Bob) Rao, Charles Young (patent atty)
Legal Department Patent Attorneys	Rob Winkle, Mark Seeley, George Chen (patent trainee)